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On Chip Communication Architectures System

Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design.

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As application complexity strains the communication backbone of SoC designs, academic and industrial R&D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architecures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures.

On-Chip Communication Architectures | ScienceDirect

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A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date ...

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Network-on-chip (NoC)-based communication architectures have emerged as an alternative to shared bus mechanism in multi-core system-on-chip (SoC) devices and the increasing number and functionality of processing cores have made such systems vulnerable to security attacks.

Secure On-Chip Communication Architecture for ...

A network on a chip or network-on-chip (NoC / □ □ n □ o□ □ s i□ / en-oh-SEE or / n □ k / knock) is a network-based communications subsystem on an integrated circuit ("microchip"), most typically between modules in a system on a chip (SoC). The modules on the IC are typically semiconductor IP cores schematizing various functions of the computer system, and are designed to be modular in ...

Network on a chip - Wikipedia

A system on a chip (SoC / □ □ s □ o□ □ s i□ / es-oh-SEE or / s □ k / sock) is an integrated circuit (also known as a "chip") that integrates all or most components of a computer or other electronic system.These components almost always include a central processing unit (CPU), memory, input/output ports and secondary storage □ all on a single substrate or microchip, the size of a coin.

System on a chip - Wikipedia

The northbridge was replaced by the system agent introduced by the Sandy Bridge microarchitecture in 2011, which essentially handles all previous Northbridge functions. Intel's Sandy Bridge processors feature full integration of northbridge functions onto the CPU chip, along with processor cores, memory controller, high speed PCI Express interface and integrated graphics processing unit (GPU).

Northbridge (computing) - Wikipedia

communication architectures system on chip interconnect a volume in systems on silicon this chapter provides an overview of various aspects of on chip communication in multiprocessor system on chips mpsocs and gives an insight into why on chip communication architectures are becoming a critical

On Chip Communication Architectures System On Chip ...

conception phase of digital systems to be highly integrated as System-on-Chips (SoC). This is especially true for digital communication systems where e.g. in the optimization of channel coding traditionally only the transmission power has been considered. In general this leads to highly complex and energy intensive receivers. Actually a proper

Chip-to-Chip and On-Chip Communications

A presentation of state-of-the-art approaches from an industrial applications perspective, Communication Architectures for Systems-on-Chip shows professionals, researchers, and students how to attack the problem of data communication in the manufacture of SoC architectures. With its lucid illustration of current trends and research improving the performance, quality, and reliability of transactions, this is an essential reference for anyone dealing with communication mechanisms for embedded ...

Communication Architectures for Systems-on-Chip - 1st ...

communication architectures are becoming a chip interconnect systems on silicon on chip communication architectures have numerous sources of delay due to signal propagation along the wires synchronization transfer modes arbitration mechanisms for congestion management cross bridge

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Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing compl. Home. Property Search. Knovel offers following tools to help you find materials and properties data. Material Property Search. Also known as Data Search, find materials and properties information from

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Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R&D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architecures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures. A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years

A presentation of state-of-the-art approaches from an industrial applications perspective, Communication Architectures for Systems-on-Chip shows professionals, researchers, and students how to attack the problem of data communication in the manufacture of SoC architectures. With its lucid illustration of current trends and research improving the performance, quality, and reliability of transactions, this is an essential reference for anyone dealing with communication mechanisms for embedded systems, systems-on-chip, and multiprocessor architectures—or trying to overcome existing limitations. Exploring architectures currently implemented in manufactured SoCs—and those being proposed—this book analyzes a wide range of applications, including: Well-established communication buses Less common networks-on-chip Modern technologies that include the use of carbon nanotubes (CNTs) Optical links used to speed up data transfer and boost both security and quality of service (QoS) The book's contributors pay special attention to newer problems, including how to protect transactions of critical on-chip information (personal data, security keys, etc.) from an external attack. They examine mechanisms, revise communication protocols involved, and analyze overall impact on system performance.

Addresses the Challenges Associated with System-on-Chip Integration Network-on-Chip: The Next Generation of System-on-Chip Integration examines the current issues restricting chip-on-chip communication efficiency, and explores Network-on-chip (NoC), a promising alternative that equips designers with the capability to produce a scalable, reusable, and high-performance communication backbone by allowing for the integration of a large number of cores on a single system-on-chip (SoC). This book provides a basic overview of topics associated with NoC-based design: communication infrastructure design, communication methodology, evaluation framework, and mapping of applications onto NoC. It details the design and evaluation of different proposed NoC structures, low-power techniques, signal integrity and reliability issues, application mapping, testing, and future trends. Utilizing examples of chips that have been implemented in industry and academia, this text presents the full architectural design of components verified through implementation in industrial CAD tools. It describes NoC research and developments, incorporates theoretical proofs strengthening the analysis procedures, and includes

algorithms used in NoC design and synthesis. In addition, it considers other upcoming NoC issues, such as low-power NoC design, signal integrity issues, NoC testing, reconfiguration, synthesis, and 3-D NoC design. This text comprises 12 chapters and covers: The evolution of NoC from SoC its research and developmental challenges NoC protocols, elaborating flow control, available network topologies, routing mechanisms, fault tolerance, quality-of-service support, and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low-power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application-specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network-on-Chip: The Next Generation of System-on-Chip Integration covers the basic topics, technology, and future trends relevant to NoC-based design, and can be used by engineers, students, and researchers and other industry professionals interested in computer architecture, embedded systems, and parallel/distributed systems.

This book provides comprehensive coverage of Network-on-Chip (NoC) security vulnerabilities and state-of-the-art countermeasures, with contributions from System-on-Chip (SoC) designers, academic researchers and hardware security experts. Readers will gain a clear understanding of the existing security solutions for on-chip communication architectures and how they can be utilized effectively to design secure and trustworthy systems.

Traditionally, design space exploration for Systems-on-Chip (SoCs) has focused on the computational aspects of the problem at hand. However, as the number of components on a single chip and their performance continue to increase, the communication architecture plays a major role in the area, performance and energy consumption of the overall system. As a result, a shift from computation-based to communication-based design becomes mandatory. Towards this end, network-on-chip (NoC) communication architectures have emerged recently as a promising alternative to classical bus and point-to-point communication architectures. In this dissertation, we study outstanding research problems related to modeling, analysis and optimization of NoC communication architectures. More precisely, we present novel design methodologies, software tools and FPGA prototypes to aid the design of application-specific NoCs.

The design of today's semiconductor chips for various applications, such as telecommunications, poses various challenges due to the complexity of these systems. These highly complex systems-on-chips demand new approaches to connect and manage the communication between on-chip processing and storage components and networks on chips (NoCs) provide a powerful solution. This book is the first to provide a unified overview of NoC technology. It includes in-depth analysis of all the on-chip communication challenges, from physical wiring implementation up to software architecture, and a complete classification of their various Network-on-Chip approaches and solutions. * Leading-edge research from world-renowned experts in academia and industry with state-of-the-art technology implementations/trends * An integrated presentation not currently available in any other book * A thorough introduction to current design methodologies and chips designed with NoCs

Abstract: Network-on-Chip (NoC) communication architectures have been recognized as the most scalable and efficient solution for on chip communication challenges in the multi-core era. Diverse demanding applications coupled with the ability to integrate billions of transistors on a single chip

are some of the main driving forces behind ever increasing performance requirements towards the level that requires several tens to over a hundred of cores per chip. Small scale multicore processors so far have been a great commercial success and found applicability in many applications. Systems using multi-core processors are now the norm rather than the exception. As the number of cores or components integrated into a single system is keep increasing, the design of on-chip communication architecture is becoming more challenging. The increasing number of components in a system translates into more inter-component communication that must be handled by the on-chip communication infrastructure. Future system-on-chip (SoC) designs require predictable, scalable and reusable on-chip communication architectures to increase reliability and productivity. Current bus-based interconnect architectures are inherently non-scalable, less adaptable for reuse and their reliability decreases with system size. NoC communication guarantees scalability, high-speed, high-bandwidth communication with minimal wiring overhead and routing issues. NoCs are layered, packet-based on-chip communication networks integrated onto a single chip. NoC consists of resources and switches that are directly connected in a way that resources are able to communicate with each other by sending messages. The proficiency of a NoC to meet its design goals and budget requirements for the target application depends on its design. Often, these design goals conflict and trade-off with each other. The multi-dimensional pull of design constraints in addition to technology scaling complicates the process of NoC design in many aspects, as they are expected to support high performance and reliability along with low cost, smaller area, less time-to-market and lower power consumption. To aid in the process, this research presents design methodologies to achieve low power and high performance NoC communication architectures for nanometer SoCs.

Sustainable Wireless Network-on-Chip Architectures focuses on developing novel Dynamic Thermal Management (DTM) and Dynamic Voltage and Frequency Scaling (DVFS) algorithms that exploit the advantages inherent in WiNoC architectures. The methodologies proposed combined with extensive experimental validation collectively represent efforts to create a sustainable NoC architecture for future many-core chips. Current research trends show a necessary paradigm shift towards green and sustainable computing. As implementing massively parallel energy-efficient CPUs and reducing resource consumption become standard, and their speed and power continuously increase, energy issues become a significant concern. The need for promoting research in sustainable computing is imperative. As hundreds of cores are integrated in a single chip, designing effective packages for dissipating maximum heat is infeasible. Moreover, technology scaling is pushing the limits of affordable cooling, thereby requiring suitable design techniques to reduce peak temperatures. Addressing thermal concerns at different design stages is critical to the success of future generation systems. DTM and DVFS appear as solutions to avoid high spatial and temporal temperature variations among NoC components, and thereby mitigate local network hotspots. Defines new complex, sustainable network-on-chip architectures to reduce network latency and energy Develops topology-agnostic dynamic thermal management and dynamic voltage and frequency scaling techniques Describes joint strategies for network- and core-level sustainability Discusses novel algorithms that exploit the advantages inherent in Wireless Network-on-Chip architectures

This book covers key concepts in the design of 2D and 3D Network-on-Chip interconnect. It highlights design challenges and discusses fundamentals of NoC technology, including architectures, algorithms and tools. Coverage focuses on topology exploration for both 2D and 3D NoCs, routing algorithms, NoC router design, NoC-based system integration, verification and testing, and NoC reliability. Case studies are used to illuminate new design methodologies.